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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/964,765	09/28/2001	Peter L. Doyle	219.40020X00	2980

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EXAMINER	
SANTIAGO, ENRIQUE L	
ART UNIT	**PAPER NUMBER**
2671	

DATE MAILED: 03/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/964,765	DOYLE ET AL.
	Examiner	Art Unit
	Enrique L Santiago	2671

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *31-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *36-41* is/are allowed.

6)☐ Claim(s) *31-35 and 42-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 31-35 and 42-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lapidous, et al. US patent no. 6,677,945 in view of Sobel et al. US patent no. 6,300,935.

-Regarding claim 31, Lapidous describes depth buffer in which a depth value is computed for a given pixel, and compared against a stored W-buffer value from the depth buffer to check for visibility (column 9, line 61 - column 10, Line 8). The values are stored in a floating-point format (column 4, lines 36-43), which is a variable format. The view volume is transformed to a normalized cube (column 7, lines 32-43), which normalizes the values of pixels in the view volume.

Lapidous does not directly teach "a register to store a value that identifies a variable format". However said apparatus is well known and in similar art Sobel et al. teaches said apparatus (see column 4, lines 26-62). Therefore it would have been obvious to one skilled in the art at the time of the invention to use said apparatus in combination with Lapidous, because it could be used to store the screen space coordinates, colors, texture coordinates, etc. processed by the polygon setup and rasterization module 1000 to prepare for pre-pixel computations (see Lapidus, fig 10, column 14, lines 23-28).

-Regarding claim 32, Lapidous describes a depth value calculation module 1010 (Fig 10) that computes the depth values of each pixel (column 14, lines 28-29).

-Regarding claim 33, Lapidous describes a decision logic module 1050 and a depth storage module 1070 (Fig 10) that receive depth values from the depth calculation module 1010 and write depth values to the buffer in the format (as determined by decision logic module 1050) of the buffer used (column 14, lines 45-49).

-Regarding claim 34, the rationale for claim 33 is incorporated. In addition, Lapidous describes a decision logic module 1050 (Fig 10) that identifies the format of the depth buffer to be used in a depth test (column 14, lines 34-40). The format of the buffer is either a 24-bit value, with 20 mantissa bits (i.e. fraction bits) and 4 exponent bits, or a 16-bit value, with 12 mantissa bits and 4 exponent bits (column 10, lines 58-68).

Lapidous does not directly teach "a register to store a value that identifies a variable format". However said apparatus is well known and in similar art Sobel et al. teaches said apparatus (see column 4, lines 26-62). Therefore it would have been obvious to one skilled in the art at the time of the invention to use said apparatus in combination with Lapidous, because it could be used to store the screen space coordinates, colors, texture coordinates, etc. processed by the polygon setup and rasterization module 1000 to prepare for pre-pixel computations (see Lapidus, fig 10, column 14, lines 23-28).

-Regarding claim 35, the rationale for claim 33 is incorporated. Additionally in Lapidous the decision logic module and depth storage module read the values stored in the buffer and provide them to the visibility-testing module 1040, and the decision logic module 1050 determines which format will be read from the buffer (column 14, lines 34-45).

-Regarding claim 42, the rationale for Claim 31 is incorporated. Lapidous also describes a display unit 1090 (Fig 10) that displays visible pixels (column 14, lines 51-54).

-Regarding claim 43, the rationale for Claim 32 is incorporated.

-Regarding to claim 44, the rationale for Claim 33 is incorporated.

-Regarding to claim 45, the rationale for Claim 34 is incorporated.

-Regarding to claim 46, the rationale for Claim 35 is incorporated.

-Regarding to claims 47-49, the rationale for Claim 41 is incorporated. The floating-point format of the W buffer is a variable format. In addition, Lapidous describes a decision logic module 1050 (Fig 10) that identifies the format of the depth buffer to be used in a depth test (Col 14 Lines 34-40). The format of the buffer is either a 24-bit value, with 20 mantissa bits (i.e. fraction bits) and 4 exponent bits, or a 16-bit value, with 12 mantissa bits and 4 exponent bits (column 10, lines 58-68).

-Regarding claim 50, Lapidous describes an embodiment of the invention wherein, if the depths of the pixels of an image (which may be a first image) are greater than a predetermined threshold, a 16-bit W buffer is used to store the depth values of the pixels (column 9, line 61 - column 10, line 4). The view volume is transformed to a normalized cube (column 7, lines 32-43), which normalizes the values of pixels in the view volume. The values are stored in a floating-point format and storing a first value indicative of the first floating point format (column 4, lines 36-43). Figure 10 illustrates a diagram of a graphics subsystem in a computer system that is designed in accordance with the invention; this subsystem may be embodied within a machine-readable medium containing instructions for a computer system.

-Regarding claim 51, in Lapidous if the depths of the pixels of another image (which may be a second image) are greater than a predetermined threshold, a 24-bit W buffer is used to store the depth values of the pixels (column 10, lines 4-8).

-Regarding claim 52, in Lapidous the format of the buffer is a floating-point number with either a 24-bit value (for the second image), with 20 mantissa bits (i.e. fraction bits) and 4 exponent bits, or a 16-bit value (for the first image), with 12 mantissa bits and 4 exponent bits (column 10, lines 58-68).

-Regarding claim 53, the rationale for claim 41 is incorporated. If the first near and far depth values associated with the first near and planes of the first image are equivalent to Zn and Zv (respectively), the equations for the threshold determining the format of the buffers ((Zv-Zn)/(Zf-Zn)=0.5, Zf/Zn=1000) have a ratio incorporating Zn and Zv. Likewise, if the second near and far depth values associated with the first near and far planes of the second image are equivalent to Zv and Zf (respectively), the equations for the threshold determining the format of the buffers have a ratio incorporating Zv and Zf.

Response to Arguments

Applicant's arguments filed January 4, 2005 regarding claims 31-35 and 42-53 have been fully considered but they are not persuasive.

In response to applicant's arguments against the references individually (i.e. page 1, second paragraph, "the official action appears to rely on Sobel..."), one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

On page 9 the applicants request that the Examiner identify "where Sobel teaches a register to store a value that identifies a variable format" As stated above the applicant is arguing against the references individually, however the references where applied in combination as stated in the rejection.

Nevertheless to satisfy the applicants request please review the following:

Lapidous describes a system wherein the values are stored in a floating-point format (see column 4, lines 36-43, column 8, line 27-column 9, line 6), which is a variable format. But as stated in the above rejection Lapidous does not directly teach "a register to store a value that identifies a variable format". However the use of registers for storing information is well known in the art. Therefore since Lapidous teaches a system, which includes the storing of values, it would have been obvious to one skilled in the art that said system would include a register as part of the storing subsystems. The register from Sobel is an example of a register that could be used in combination with Lapidous. Further in the applicants disclosure there is no specific register used, the applicant merely states in paragraph [0047] "*The number of fraction bits in the variable-formatable floating point number may be stored within a register (such as in the graphics controller 140 and communicated to the appropriate hardware such as the depth buffer)*" and since Lapidous teaches the use of a depth buffer for storing and retrieving data (see the abstract) it would have been obvious to one skilled in the art that Lapidous would include "registers" and a "graphics controller" to perform the previously stated function, therefore the combination is proper and the rejection of claims 31-35 and 42-53 is affirmed.

Applicant's arguments filed January 4, 2005 regarding claims 36-41 have been fully considered and they are persuasive.

Allowable Subject Matter

Claims 36-41 are allowed.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US patent no. 5,808,618

US patent no. 5,629,769

US patent no. 4,563,548

US patent no. 4,257,096

Article: "Optimal Depth Buffer for low-Cost Graphics Hardware", by Eugene Lapidous*, Guofang Jiao*, Trident Microsystems Inc., pages 67-73, *2450 Walsh Avenue, Santa Clara CA 95051, ACM 1999 1-58113-170-4/99/08.

Definition of W-Buffer, Smart Computing (online)

http://www.smartcomputing.com/

Definition of Buffer, Dictionary of Computers (on line)

http://www.tiscali.co.uk/reference/dictionaries/computers/data/content_a.html

Definition of Register, Dictionary of Computers (on line)

http://www.tiscali.co.uk/reference/dictionaries/computers/data/content_a.html

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enrique L Santiago whose telephone number is (571) 272-7648. The examiner can normally be reached on Monday to Friday from 7:00 A.M. to 3:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Zimmerman whose telephone number is (571) 272-7653, can be reached on Monday to Friday from 7:00 A.M. to 3:30 P.M.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

703 872-9306 (for Technology Center 2600 only)

Hand-delivered responses should be brought to [Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor] (Receptionist).

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Enrique L. Santiago

March 11, 2005

MARK ZIMMERMAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600